CLAIMS

1. A method of designing an essentially digital system (EDS) which executes at least one system task, comprising:

inputting a system-level description of a functionality of the EDS including design parameters of the EDS for executing the system task;

providing a first library of descriptions of hardware components, at least some of the hardware components being suitable for use in the EDS and each being suitable for executing a component task, at least a first group and a second group of components being at least partly made by semiconductor processing, wherein the manufacture of the first component group has at least one different semiconductor processing step compared with the manufacture of the second component group, the first library being structured such that for each of the first and second groups of components, performance parameters are accessible, performance parameters being at least a cost function and a constraint related to executing the component task;

deriving from the first library two or more components from the first and/or second group belonging to a first trade-off set, each component belonging to the first trade-off set having a cost function-constraint combination, wherein any first combination within the first trade-off set is configured such that all combinations within the first trade-off set, having a cost function with a lower cost value than the first combination, have a higher value of the constraint than the first combination and such that all combinations within the first trade-off set, having a value of the constraint lower than that of the first combination, have a higher value of the cost function than that of the first combination; and

constructing at least one design of the EDS compatible with the high level description from one or more components of the trade-off set.

2. The method according to claim 1, further comprising:

providing a second library of descriptions of first and second hardware sub-components, at least some of the hardware sub-components being suitable for use in the first and/or second hardware components and each sub-component having at least two performance parameters, the at least two performance parameters including a second constraint and a second cost function, at least a third group and a fourth group of sub-components being at least partly made by a semiconductor processing and the

manufacture of the third sub-component group having at least one different semiconductor processing step compared with the manufacture of the fourth sub-component group, the second library being structured such that for each of the third and fourth groups of sub-components the performance parameters are accessible; and

deriving the first library from the second library by selecting two or more sub-components from the third and/or fourth group belonging to a second trade-off set for designing the components of the first and second group, each sub-component belonging to the second trade-off set having a cost function-constraint combination,

wherein any first combination within the second trade-off set is configured such that all combinations within the second trade-off set, having a cost function with a lower cost value than the first combination, have a higher value of the constraint than the first combination and that all combinations within the second trade-off set, having a value of the constraint lower than that of the first combination, have a higher energy consumption than that of the first combination.

3. The method according to claim 1, wherein the first trade-off set is Pareto optimized.

4. The method according to claim 2, wherein the second trade-off set is Pareto optimized.

5. The method according to claim 1, wherein the cost function includes at least one of the following: energy consumption, power and quality degradation.

6. The method according to claim 2, wherein the cost function includes at least one of the following: energy consumption, power and quality degradation.

7. The method according to claim 1, wherein the constraint includes at least one of the following: execution rate, bandwidth and latency.

8. The method according to claim 2, wherein the constraint includes at least one of the following: execution rate, bandwidth and latency

9. The method according to claim 1, wherein the semiconductor processing step includes at least one of the following: forming a conducting line width and/or length, using a material for a conductive or an insulating element, forming an aspect ratio of a conducting element, forming spacing of conducting elements, doping a semiconductor region, forming a transistor gate length and forming a transistor gate oxide thickness.

10. The method according to claim 2 wherein the sub-component includes at least one of the following: a conducting line or element, a material for a conductive or an insulating element, an array of at least two conducting elements spaced apart, a doped semiconductor region, a transistor, a transistor gate, a transistor gate oxide, a resistor, a capacitor and an inductor.

11. The method according to claim 1, wherein the component includes at least one of the following: a storage device, a memory, an FPGA, a PLA, a PAL, a microprocessor, a co-processor, a digital signal processing (DSP) circuit, a pipeline, a hardware accelerator, a driver circuit, a modem and an I/O interface circuit.

12. The method according to claim 1, wherein the design parameters include at least energy consumption when executing the system task and a rate of execution of the system task

13. A method of designing an essentially digital system (EDS) which executes at least one system task, comprising:

inputting a system-level description of a functionality of the EDS including design parameters of the EDS for executing the system task;

providing a first library of descriptions of hardware components, at least some of the hardware components being suitable for use in the EDS and each being suitable for executing a component task, at least a first group and a second group of components being at least partly made by semiconductor processing, wherein the manufacture of the first component group has at least one different semiconductor processing step compared with the manufacture of the second component group, the first library being structured such that for each of the first and second groups of components, performance parameters are accessible, performance parameters being at

least a first costs function and a second constraint when executing the component task;

providing a second library of descriptions of first and second hardware sub-components, at least some of the hardware sub-components being suitable for use in the first and/or second hardware components and each sub-component having at least two performance parameters, the performance parameters including at least a second cost function and at least a second constraint, at least a third group and a fourth group of sub- components being at least partly made by a semiconductor processing and the manufacture of the third sub-component group having at least one different semiconductor processing step compared with the manufacture of the fourth sub-component group, the second library being structured such that for each of the third and fourth groups of sub-components the performance parameters are accessible;

wherein providing the first library comprises deriving the first library from the second library by selecting two or more sub-components from the third and/or fourth group belonging to a first trade-off set for the design of the components of the first and second group, each sub-component of the trade-off set having a second cost-constraint combination;

deriving from the first library two or more components from the first and/or second group belonging to a second trade-off set, each component of the trade-off set having a first cost-constraint combination, and

constructing at least one design of the EDS compatible with the high level description from one or more components of the second trade-off set.

14. The method according to claim 13, wherein at least one of the first and second trade-off sets is Pareto optimized.

15. The method according to claim 13, wherein the cost function includes at least one of the following: energy consumption, power and quality degradation.

16. The method according to claim 13, wherein the constraint includes at least one of the following: execution rate, bandwidth and latency.

17. The method according to claim 13, wherein the semiconductor processing step includes at least one of the following: forming a conducting line width and/or length,

using a material for a conductive or an insulating element, forming an aspect ratio of a conducting element, forming spacing of conducting elements, doping a semiconductor region, forming a transistor gate length and forming a transistor gate oxide thickness.

18. The method according to claim 13, wherein the sub-component includes at least one of the following: a conducting line or element, a material for a conductive or an insulating element, an array of at least two conducting elements spaced apart, a doped semiconductor region, a transistor, a transistor gate, a transistor gate oxide, a resistor, a capacitor and an inductor.

19. The method according to claim 13, wherein the component includes at least one of the following: a storage device, a memory, an FPGA, a PLA, a PAL, a microprocessor, a co-processor, a digital signal processing (DSP) circuit, a pipeline, hardware accelerator, a driver circuit, a modem and an I/O interface circuit.

20. The method according to claim 13, wherein the design parameters are at least energy consumption when executing the system task and a rate of execution of the system task

21. The method according to claim 13, wherein the system task is a data dominated task.

22. The method according to claim 13, wherein the system task includes at least one of the following: displaying a visible image or reproducing a audio tone, coding or encoding a digital bit stream or digital data, compressing or decompressing a digital bit stream or digital data, modulation and demodulation of a signal.

23. The method according to claim 13, wherein the constructing comprises constructing the design of the EDS compatible with the high level description having at least first and second components of the trade-off set, each being for execution of a task, and designing an operating system for the EDS such that the EDS is for execution of a first and a second behavior, and the operating system has means for selecting one of the first and second components for execution of both the first and second behavior,

each of the first and second components being able to execute each of the first and second behaviors at a plurality of operating points belonging to a third trade-off set, each operating point relating to a constraint-cost combination.

24. An apparatus for designing an essentially digital system (EDS) which executes at least one system task, the apparatus comprising:

a processing unit co-operating with a first and a second essentially digital hardware device (EDHD), each of the first and second EDHDs being at least partly made by semiconductor processing, wherein the manufacture of the first EDHD has at least one different semiconductor processing procedure compared with the manufacture of the second EDHD; and

a selecting unit configured to select one of the first and second EDHDs for execution of first and second behaviors, each of the first and second EDHDs executing each of the first and second behaviors at a plurality of operating points belonging to a trade-off set, each operating point relating to a constraint-cost combination,

wherein any first combination within the trade-off set is configured such that all combinations within the trade-off set, having a cost function with a lower cost value than the first combination, have a higher value of the constraint than the first combination and such that all combinations within the trade-off set, having a value of the constraint lower than that of the first combination, have a higher value of the cost function than that of the first combination.

25. The apparatus of Claim 24, wherein the selecting unit is implemented in an operating system of the apparatus.

26. The apparatus of Claim 24, wherein the EDHD includes at least one of the following: a memory, a microprocessor, a co-processor, an FPGA, a PLA, a PAL, a digital signal processing (DSP) circuit, a pipeline, a hardware accelerator, a driver circuit, a modem and an I/O interface circuit.

27. The apparatus of Claim 24, wherein the trade-off set is preferably Pareto optimized.

28. An essentially digital system (EDS) designed by a method, wherein the method comprises:

inputting a system-level description of a functionality of the EDS including design parameters of the EDS for executing at least one system task;

providing a first library of descriptions of hardware components, at least some of the hardware components being suitable for use in the EDS and each being suitable for executing a component task, at least a first group and a second group of components being at least partly made by semiconductor processing, wherein the manufacture of the first component group has at least one different semiconductor processing step compared with the manufacture of the second component group, the first library being structured such that for each of the first and second groups of components, performance parameters are accessible, performance parameters being at least a cost function and a constraint related to executing the component task;

deriving from the first library two or more components from the first and/or second group belonging to a first trade-off set, each component belonging to the first trade-off set having a cost function-constraint combination, wherein any first combination within the first trade-off set is configured such that all combinations within the first trade-off set, having a cost function with a lower cost value than the first combination, have a higher value of the constraint than the first combination and such that all combinations within the first trade-off set, having a value of the constraint lower than that of the first combination, have a higher value of the cost function than that of the first combination; and

constructing at least one design of the EDS compatible with the high level description from one or more components of the trade-off set.

29. A computer readable medium storing executable codes, wherein the codes are configured to design an essentially digital system (EDS) which executes at least one system task, wherein the medium comprises:

a code configured to input a system-level description of a functionality of the EDS including design parameters of the EDS for executing at least one system task;

a code configured to provide a first library of descriptions of hardware components, at least some of the hardware components being suitable for use in the EDS and each being suitable for executing a component task, at least a first group and

a second group of components being at least partly made by semiconductor processing, wherein the manufacture of the first component group has at least one different semiconductor processing step compared with the manufacture of the second component group, the first library being structured such that for each of the first and second groups of components, performance parameters are accessible, performance parameters being at least a cost function and a constraint related to executing the component task;

a code configured to derive from the first library two or more components from the first and/or second group belonging to a first trade-off set, each component belonging to the first trade-off set having a cost function-constraint combination, wherein any first combination within the first trade-off set is configured such that all combinations within the first trade-off set, having a cost function with a lower cost value than the first combination, have a higher value of the constraint than the first combination and such that all combinations within the first trade-off set, having a value of the constraint lower than that of the first combination, have a higher value of the cost function than that of the first combination; and

a code configured to construct at least one design of the EDS compatible with the high level description from one or more components of the trade-off set.